ZHENYI SHEN

(+86)13913099056 | zhenyi.shen16@alumni.imperial.ac.uk | https://www.zhenyishen.com/

EDUCATION

Imperial College London **London, UK**

Master of Engineering in Electrical and Electronic **10.2016–7.2020**

- Achieved First Class Honour, ranking the top 20% overall (Dean's List 2016).
- Related Courses: Machine Learning, Pattern recognition, Deep Learning, Computer Vision, Speech Processing, Optimisation, Signal Processing, Wavelets, Probability and Stochastic Processing, Linear Algebra and more.
- Completed over 20 labs and courseworks with 4 out of 5 in Computer Vision and Pattern Recognition receiving A* grades.

WORK EXPERIENCES

iFLYTEK Co. Ltd. **12.2021–Present**

Speech Synthesis Engineer *Shanghai, China*

Led the development of speech synthesis capabilities across diverse Chinese dialects and ethnic languages.

- Engineered low-resource language speech synthesis including Taiwanese Mandarin, Suzhou dialect, Shanghai dialect, and Southern Min language, all of which obtained a Mean Opinion Score (MOS) above 4.0 — indicating high-quality audio perception by human listeners and marking a top-tier performance in the global market.
- Conducted in-depth research on a common text-analysis/NLU module across dialects in speech synthesis, optimising the overall rhythm and intonation adjustments of synthesised audio across dialects, enhancing the controllability and robustness of the dialect Text-to-Speech system.

Zhuofan Information Technology Co. Ltd. **8.2020–12.2021**

Computer Vision Engineer *Shanghai, China*

Leveraged computer vision technologies to enhance E-Government IT solutions, thereby automating administrative tasks such as surveillance, customer registration, and licence issuance.

- Developed a sophisticated real-time facial recognition platform, central to the surveillance scheme.
- Engineered a document classification system with extensive data augmentation capabilities and hyperparameter optimisation for simplified deployment across diverse specs by non-tech users. The end product was showcased at the World Artificial Intelligence Conference 2021.

MediaTek Inc. **4.2019–10.2019**

Verification Engineer Intern, Supervisor: Dr. Dimitris Nalbantis *Kent, UK*

- Completed the functional verification of MediaTek's next-gen 5G cellular RFIC via unit testing and integration testing all simulated modules, while gaining hands-on experience and proficiency in RFIC verification on a top-tier team.

RESEARCH EXPERIENCES

Temporally Coded Spiking Neural Networks **10.2019–6.2020**

Imperial College London, Supervisors: Professor Pier Luigi Dragotti and Mr. Vincent C.H. Leung *London, UK*

- Researched on temporally-coded SNNs (Spiking Neural Networks), developing a PyTorch implementation and analysing its potential on real-world datasets like N-MNIST and DVS-128. The project explored an innovative architecture combining temporally-coded SNN and the state-of-the-art rate-coded SNNs sequentially through a converter module, aiming the obtain both the high performance of rate-coded SNNs and the computational efficiency of the temporally-coded ones.

Undergraduate Research Opportunity **6.2018–9.2018**

Imperial College London, Supervisors: Professor George A. Constantinides and Dr. James J. Davis *London, UK*

- Engineered an FPGA-based device checker, capable of determining the failure frequency of on-chip device, testing up to an upper limit of 800MHz with negligible error margins.

SKILLS

- **Programming**: Proficient in Python (PyTorch, NumPy, spaCy, HuggingFace Transformers), Bash, LATEX; Experience with MATLAB, Verilog, C++, Prolog.
- **Languages**: Fluent in English (IELTS: 7.5), and native in Mandarin.